Image & AF 2812

ATTORNEY DOCKET NO.: CHOI 30-10-5-4-13 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of: Seungmoo Choi, *et al.*

Serial No.: 10/038,734

Filed: December 31, 2001

For: METHOD FOR FABRICATING MOS DEVICE WITH HALO IMPLANTED REGION

Grp./A.U.: 2812

Examiner: Booth, Richard A.

CERTIFICATE OF FIRST CLASS MAILING

I hereby certify that this correspondence, including the attachments listed, is being deposited as First Class Mail with the United States Postal Service, in an envelope addressed to Commissioner of Patents, Alexandria, VA 22313-1450, on the date shown below.

February 6, 2004 Elizabeth Schumacher
Date of Mailing Signature of person mailing

Commissioner for Patents
Washington, D. C. 20231

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ATTENTION: Board of Patent Appeals and Interferences

Sirs:

APPELLANT'S BRIEF UNDER 37 C.F.R. §1.192

This is an appeal from a Final Rejection dated August 21, 2003, of Claims 15-19 and 21-30. The Appellant submits this Brief in triplicate as required by 37 C.F.R. §1.192(a), with the statutory fee of $ 320.00 as set forth in 37 C.F.R.§1.17(c), and hereby authorizes the Commissioner to charge

any additional fees connected with this communication or credit any overpayment to Deposit Account No. 08-2395.

This Brief contains these items under the following headings, and in the order set forth below in accordance with 37 C.F.R. §1.192(c):

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is the Assignee, Agere Systems, Inc.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

III. STATUS OF THE CLAIMS

The Appellants originally filed Claims 1-20. Claims 15-19 were reintroduced in the present application, filed as a divisional. The Appellants added new Claims 21-30 by amendment. Therefore, Claims 15-19 and 21-30 are pending and currently stand rejected with no claims objected to or allowed. Claims 15-19 and 21-30 are being appealed.

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On September 26, 2002, the Appellant filed an amendment to Claim 15 and added Claims 21-30. On June 11, 2003 the Appellant amended Claims 15, 24 and 25. By office action mailed August 21, 2003, the Examiner issued a final rejection of Claims 15-19 and 21-30. After response by Appellant, the Examiner issued an advisory action dated November 3, 2003, that the response by Appellant did not place the application in condition for allowance. On November 10, 2003, the Appellant filed a Notice of Appeal.

V. SUMMARY OF THE INVENTION

Among other things, the present invention provides for a metal-oxide-semiconductor (MOS) device 10 with a contoured halo implant 42, 44. As shown in Illustration 1, which is Figure 1 of the present application, set forth below, the device includes a gate structure 22 on a semiconductor substrate 12. Over the gate structure 22 is an upper layer of a hard mask 60 material that is contoured such that it varies in thickness across the gate structure 22. The thickness of the hard mask 60 terminates at the periphery of the gate structure 22. Located under the gate structure 22,

in the semiconductor substrate 22, is a halo implant 42, 44 with a depth profile 46,48 that follows at least a portion of the contour of the hard mask 60 layer overlying the gate structure 22.

FIG. 1

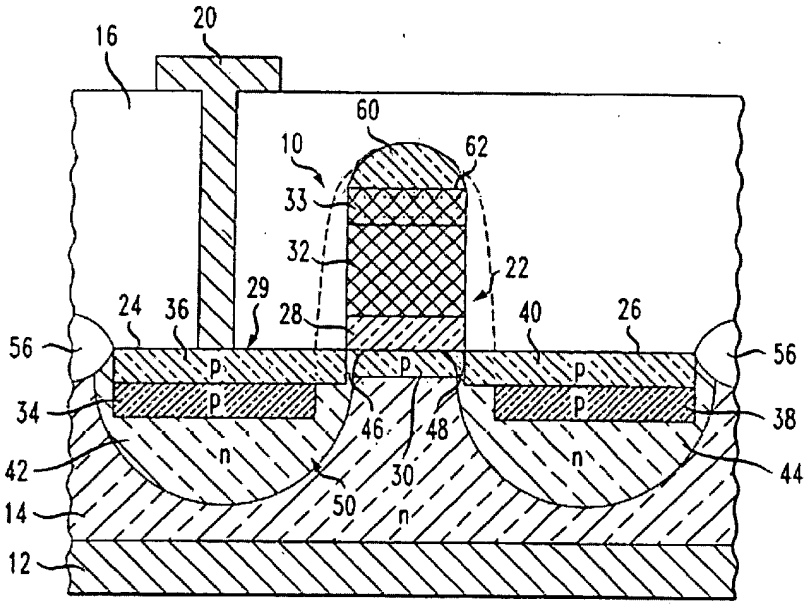


Illustration 1

VI. ISSUES

1. Whether Claims 15, 17-18, 21-24, and 27-28 are unpatentable under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,458,656 to Park *et al.* (Park).

2. Whether Claims 16 and 26 are unpatentable under 35 U.S.C. §103(a) as being obvious over Park.

3. Whether Claims 19 and 29-30 are unpatentable under 35 U.S.C. §103(a) as being obvious over Park in view of U.S. Patent No. 5,776,811 to Wang *et al.* (Wang).

VII. GROUPING OF THE CLAIMS

Claims 15-19 and 21-30 stand or fall together.

IX. THE APPELLANT'S ARGUMENTS

1. Anticipation by Park.

The Examiner determined that independent Claim 15 and dependent Claims 17-18, 21-24, and 27-28 are unpatentable under 35 U.S.C. §102(e) as being anticipated by Park. The Appellant respectfully submits that Park does not use a halo implant that follows at least a portion of a contour of a hardmask, where the thickness of the hardmask varies across the gate structure and terminates at a periphery of the gate structure. Referring to Illustration 2 below, which is Figure 5 from Park, Park is directed to a process of fabricating a two bit EEPROM device that uses an ONO layer 24 and a photoresist 34 to implant p-type regions 44 into the substrate 23. The ONO 24 layer is first

patterned with the photoresist 34 followed by which an n-type region 46 is implanted into the substrate 23 through the opening. Following this implantation step, the photoresist 34 is subjected to a flow operation that rounds the corners. An angled p-type implantation process 62 is then conducted through the same opening used to form the n-type region 46 to form p-type 44regions near the edges of the ONO layer 24. (Column 6, lines 20-66).

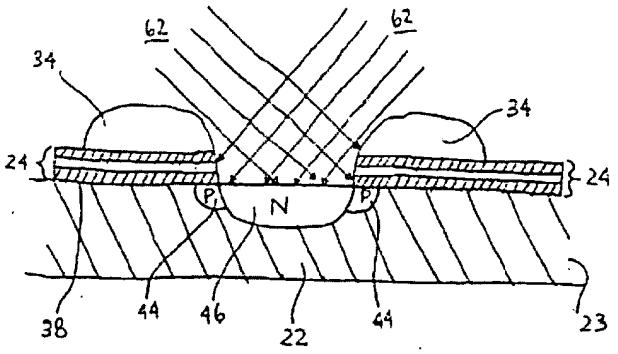


Illustration 2

Park does not anticipate several aspects of the presently claimed invention. First, the contour of the resulting p-type 44 implant does not follow the contour of at least a portion of the hardmask 34, as recited in the pending claims. To the contrary, the contour of the p-type implant is the opposite or reciprocal of the photoresist 34, as easily seen from Illustration 2. Second, the photoresist 34 is not located on a gate structure, but is instead, located on an ONO layer 24 over which a gate structure will be deposited after the implantation and oxidation processes. Thus, the thickness of the photoresist cannot vary across the gate structure and terminate at a periphery of the gate structure because there is no gate structure. Furthermore, the photoresist is ultimately removed,

and thus, the final MOS device taught by Park will not include the photoresist layer, which functions as a mask layer in Park. (Column 7, lines 9-12). Accordingly, Park fails to disclose each and every element of independent Claim 15 or dependent Claims 17-18, 21-24 and 27-28 and, therefore, does not anticipate the claimed invention under 35 U.S.C. §102(e). Accordingly, the Appellant respectfully requests that the Board of Patent Appeals and Interferences reverse the Examiner's Final Rejection of the Appellant's pending Claims 15, 17-18, 21-24 and 27-28

2. Obvious over Park

The Examiner rejected Claims 16 and 26 as obvious over Park and, therefore, unpatentable under 35 U.S.C. §103. However, as discussed above, Park fails to teach several of the elements of Claim 15 on which Claims 16 and 26 depend. Furthermore there is no suggestion in Park that would lead one of ordinary skill in the pertinent art to arrive at such a structure. The implantation of the p-type region 44 is carefully conducted to form them at the edges of the ONO layer 24 to achieve a high density device. (Column 3, lines 49-64). The resulting structure is the one illustrated above in Illustration 2, and as explained above, it does not result in an implant that follows at least a portion of the contour of the photoresist. Given the explicit teaching in Park on how to achieve this implant, one who is skilled in the art would not be motivated to arrive at the implant as presently recited in these dependent claims without using the present application as a blueprint. Additionally, there is no teaching or suggestion of forming the photoresist on the gate structure because given the implicit teachings of Park, the gate is formed subsequent to the implantation and removal of the photoresist. There is also no motivation for one skilled in the art to conduct the implants subsequent to the gate formation without turning to non-obvious modifications of the process steps. Furthermore, given

the fact that Park teaches removing the photoresist, one who is skilled in the art would not be motivated to leave the photoresist on the gate upon completing the MOS device. Therefore, Park fails to teach or suggest each and every element of Claims 16 and 26, and as such, fails to establish a *prima facie* case of obviousness regarding these claims. Accordingly, the Appellant respectfully requests that the Board of Patent Appeals and Interferences reverse the Examiner's Final Rejection of the Appellant's pending Claims 16 and 26.

3. Obvious over Park in view of Wang

The Examiner rejected Claims 19 and 29-30 as obvious over Park in view of Wang and, therefore, unpatentable under 35 U.S.C. §103. Wang describes a simplified fabrication procedure for making flash EEPROM memory cells. The method described comprises performing a double-diffuse (deep) junction implant after the shallow source/drain of the memory cell have been implanted and formed. A high energy double-diffuse implant is used to replace separate, individual implant and diffusion steps which results in a memory cell having less damage to its substrate. One embodiment as disclosed in Wang is shown below in Illustration 3.

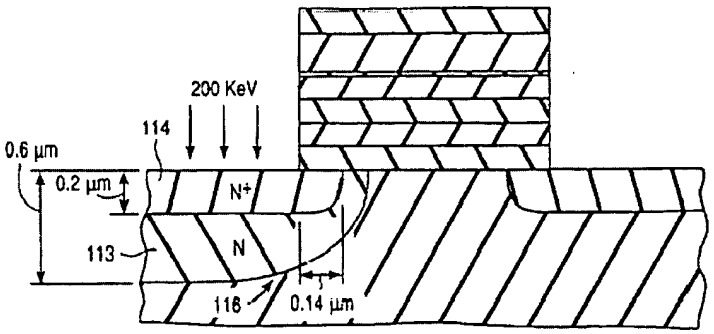


Illustration 3

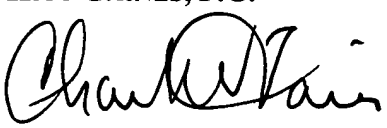
Thus as seen from Illustration 3, above, Wang describes a simplified fabrication procedure for making flash EEPROM memory cells. The method described comprises performing a non-angled double-diffuse (deep) junction implant after the shallow source/drain of the memory cell have been implanted and formed. A high energy double-diffuse implant is used to replace separate, individual implant and diffusion steps which results in a memory cell having less damage to its substrate.

Wang fails to cure the deficient teachings of Park, discussed above, inasmuch as there is no teaching or suggestion in Wang of a hardmask as recited in Claim 15, on which Claims 19 and 29-30 depend. Furthermore, one who is skilled in the art would not be motivated to add a mask to the teachings of Wang because to do so would require extensive changes to the process that would add not only unforeseeable variables to the process, but also add to the cost of production, both of which the industry attempts to avoid. Therefore, the combination of Park and Wang fails to teach or suggest each and every element of Claims 19 and 29-30, and as such, fails to establish a *prima facie* case of obviousness regarding these claims.

Accordingly, the Appellant respectfully requests that the Board of Patent Appeals and Interferences reverse the Examiner's Final Rejection of the Appellant's pending claims 19 and 29-30.

Respectfully submitted,

HITT GAINES, P.C.



Charles W. Gaines
Registration No. 36,804

Dated: 2/6/04

P.O. Box 832570
Richardson, Texas 75083
(972) 480-8800
(972) 480-8865 (Fax)

X. APPENDIX A - CLAIMS

15. A MOS device comprising:

a gate structure on a semiconductor substrate, the gate structure having an upper layer of a hard mask material, the hard mask material being contoured such that it varies in thickness across the gate structure, and wherein the thickness of the hard mask terminates at a periphery of the gate structure; and

a halo implant in the semiconductor substrate, the halo implant having a depth profile under the gate structure which follows at least a portion of the contour of the hard mask layer.

16. The device of Claim 15, wherein the hard mask is a layer of silicon.

17. The device of Claim 15, wherein the hard mask layer has a convex upper surface.

18. The device of Claim 15, wherein the halo implant is formed by a process which includes implanting a halo dopant into the substrate through the hard mask material at an implant angle which is generally perpendicular to the surface of the substrate.

19. The device of Claim 15, wherein the gate structure includes a layer of polysilicon.

21. The device of Claim 15 wherein the hard mask layer is substantially dome-shaped.

22. The device of Claim 15 wherein the hard mask layer contour has a top portion and side portions, wherein the depth profile of the halo implant under the gate structure follows the side portions of the hard mask layer contour.

23. The device of Claim 22 further including a channel defined between regions of the halo implant, the regions defined by the depth profile following the side portions of the hard mask layer.

24. The device of Claim 15 wherein the hard mask has a maximum thickness at a mid-point thereof and a minimum thickness at a periphery thereof

25. The device of Claim 24 further including spacers located on the sides of the gate structure and contacting the hard mask within the periphery of the gate structure.

26. The device of claim 15 wherein a depth of the halo implant under an edge of the gate structure is substantially equal to a maximum thickness of the hard mask layer.

27. The device of Claim 15 wherein the depth of the halo implant is substantially zero under a midpoint of the hard mask layer.

28. The device of Claim 27 wherein the depth of the halo implant is zero under the midpoint of the hard mask layer.

29. The device of Claim 15 wherein the gate structure includes a layer of tungsten silicide between the hard mask layer and the substrate.

30. The device of Claim 15 wherein the gate structure includes a layer of polycide between the hard mask layer and the substrate.

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February 6, 2004 Elizabeth Shumaker
Date of Mailing Signature of person mailing

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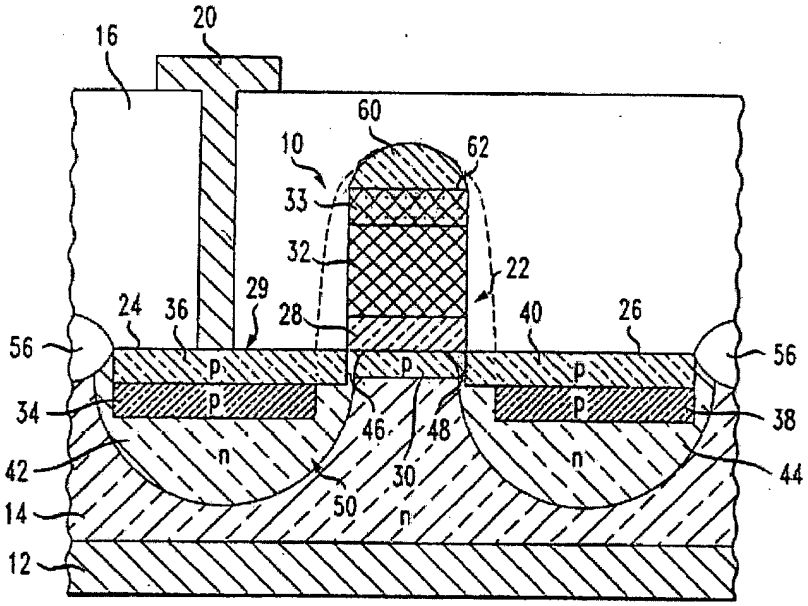

Illustration 1

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patterned with the photoresist 34 followed by which an n-type region 46 is implanted into the substrate 23 through the opening. Following this implantation step, the photoresist 34 is subjected to a flow operation that rounds the corners. An angled p-type implantation process 62 is then conducted through the same opening used to form the n-type region 46 to form p-type 44regions near the edges of the ONO layer 24. (Column 6, lines 20-66).

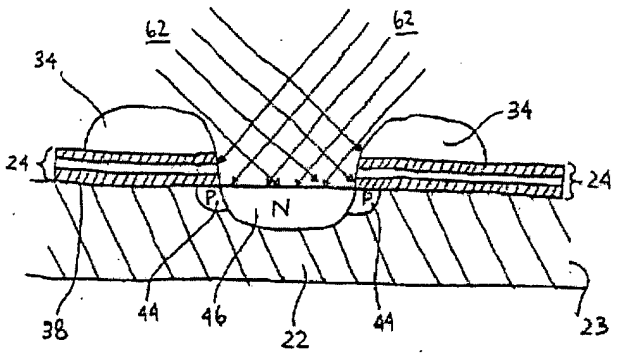

Illustration 2

Park does not anticipate several aspects of the presently claimed invention. First, the contour of the resulting p-type 44 implant does not follow the contour of at least a portion of the hardmask 34, as recited in the pending claims. To the contrary, the contour of the p-type implant is the opposite or reciprocal of the photoresist 34, as easily seen from Illustration 2. Second, the photoresist 34 is not located on a gate structure, but is instead, located on an ONO layer 24 over which a gate structure will be deposited after the implantation and oxidation processes. Thus, the thickness of the photoresist cannot vary across the gate structure and terminate at a periphery of the gate structure because there is no gate structure. Furthermore, the photoresist is ultimately removed,

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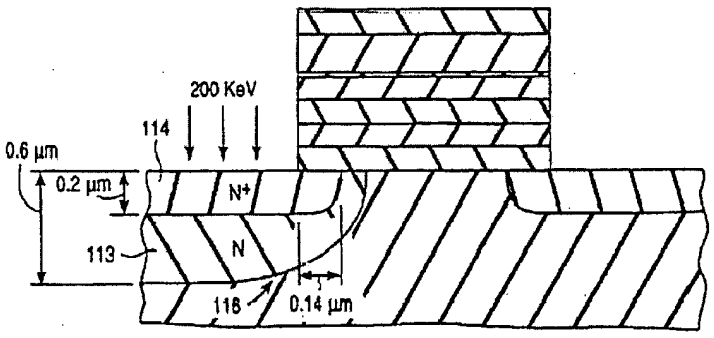

Illustration 3

Thus as seen from Illustration 3, above, Wang describes a simplified fabrication procedure for making flash EEPROM memory cells. The method described comprises performing a non-angled double-diffuse (deep) junction implant after the shallow source/drain of the memory cell have been implanted and formed. A high energy double-diffuse implant is used to replace separate, individual implant and diffusion steps which results in a memory cell having less damage to its substrate.

Wang fails to cure the deficient teachings of Park, discussed above, inasmuch as there is no teaching or suggestion in Wang of a hardmask as recited in Claim 15, on which Claims 19 and 29-30 depend. Furthermore, one who is skilled in the art would not be motivated to add a mask to the teachings of Wang because to do so would require extensive changes to the process that would add not only unforeseeable variables to the process, but also add to the cost of production, both of which the industry attempts to avoid. Therefore, the combination of Park and Wang fails to teach or suggest each and every element of Claims 19 and 29-30, and as such, fails to establish a *prima facie* case of obviousness regarding these claims.

Accordingly, the Appellant respectfully requests that the Board of Patent Appeals and Interferences reverse the Examiner's Final Rejection of the Appellant's pending claims 19 and 29-30.

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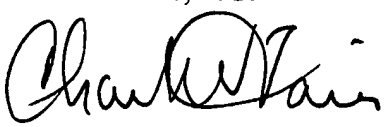
HITT GAINES, P.C.



Charles W. Gaines
Registration No. 36,804

Dated: 2/6/04

P.O. Box 832570
Richardson, Texas 75083
(972) 480-8800
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X. APPENDIX A - CLAIMS

15. A MOS device comprising:

a gate structure on a semiconductor substrate, the gate structure having an upper layer of a hard mask material, the hard mask material being contoured such that it varies in thickness across the gate structure, and wherein the thickness of the hard mask terminates at a periphery of the gate structure; and

a halo implant in the semiconductor substrate, the halo implant having a depth profile under the gate structure which follows at least a portion of the contour of the hard mask layer.

16. The device of Claim 15, wherein the hard mask is a layer of silicon.

17. The device of Claim 15, wherein the hard mask layer has a convex upper surface.

18. The device of Claim 15, wherein the halo implant is formed by a process which includes implanting a halo dopant into the substrate through the hard mask material at an implant angle which is generally perpendicular to the surface of the substrate.

19. The device of Claim 15, wherein the gate structure includes a layer of polysilicon.

21. The device of Claim 15 wherein the hard mask layer is substantially dome-shaped.

22. The device of Claim 15 wherein the hard mask layer contour has a top portion and side portions, wherein the depth profile of the halo implant under the gate structure follows the side portions of the hard mask layer contour.

23. The device of Claim 22 further including a channel defined between regions of the halo implant, the regions defined by the depth profile following the side portions of the hard mask layer.

24. The device of Claim 15 wherein the hard mask has a maximum thickness at a mid-point thereof and a minimum thickness at a periphery thereof

25. The device of Claim 24 further including spacers located on the sides of the gate structure and contacting the hard mask within the periphery of the gate structure.

26. The device of claim 15 wherein a depth of the halo implant under an edge of the gate structure is substantially equal to a maximum thickness of the hard mask layer.

27. The device of Claim 15 wherein the depth of the halo implant is substantially zero under a midpoint of the hard mask layer.

28. The device of Claim 27 wherein the depth of the halo implant is zero under the midpoint of the hard mask layer.

29. The device of Claim 15 wherein the gate structure includes a layer of tungsten silicide between the hard mask layer and the substrate.

30. The device of Claim 15 wherein the gate structure includes a layer of polycide between the hard mask layer and the substrate.